AMENDMENTS TO THE CLAIMS:

1.(original): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for segmenting an address of said packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a block basis.

2.(original): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of

scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for temporarily writing the packets to a multicast-oriented memory for multicasting to a plurality of output lines, reading the packets corresponding to the number of multicasts, with a scheme to distribute the packets to a desired FIFO memory, retaining the number of multicasts and addresses thereof according to the addresses after being distributed in order to logically actualize the distribution of not the packets but by use of only the addresses, and thus making an address management of said packet buffer memory unit.

3.(currently amended): A packet switch according to claim 1, wherein said address management unit manages sequence numbers pointing to the addresses in the block and ~~the addresses by~~ flags indicating which data of the addresses pointed to by each sequence number in the block ~~and which address related to this indicated sequence number~~ a multicast is completed with.

4.(currently amended): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit having ~~A packet switch according to claim 1, wherein said packet buffer memory unit has~~ a large-capacity memory that is high-speed accessible only when in a burst access and is disposed at a front stage, and a high-speed random accessible memory disposed at a rear stage, for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets, wherein only said rear-stage memory is normally used, when said rear-stage memory is full of packet data, the packet data are temporarily stored in said front-stage memory, and the packet data are transferred back to said rear-stage memory when a free area comes out,

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for segmenting an address of said packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a

block basis.

5.(currently amended): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit having ~~A packet switch according to claim 1, wherein said packet buffer memory unit has~~ a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a large-capacity low-speed access memory disposed in parallel at a rear stage, for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets, wherein a writing operation to said rear-stage memory is effected in parallel from said front-stage memory, and a reading operation from said rear-stage memory is effected by selecting only a queue memory with no conflict,

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for segmenting an address of said packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a

block basis.

6.(currently amended): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit having ~~A packet switch according to claim 1, wherein said packet buffer memory unit has~~ a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a queue memory using a large-capacity memory that is high-speed accessible only when in a burst access and disposed at a rear stage, for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets, wherein a writing operation to said rear-stage memory is effected batchwise just when a plurality of packets are accumulated in said front-stage memory, and the plurality of packets are read batchwise from said rear-stage memory,

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for segmenting an address of said packet buffer

memory unit into fixed-length blocks for a plurality of packets, and managing the address on a block basis.

7.(previously presented): A packet switch according to claim 1, wherein said packet buffer memory executes time-division-multiplexing of the fixed-length packets of the plurality of input lines onto one signal input line in an established manner, and includes memories disposed in parallel corresponding to every input line before being multiplexed, and

the writing and reading to and from said respective memories are executed in parallel.

8.(previously presented): A packet switch according to claim 1, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

9.(previously presented): A packet switch according to claim 1, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

10.(currently amended): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for segmenting an address of said packet buffer memory unit into fixed-length blocks for a plurality of packets, and managing the address on a block basis, ~~A packet switch according to claim 1,~~

wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided, and

the switching can be thereby done when in maintenance and in fault.

11.(original): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory unit has a large-capacity memory that is high-speed accessible only when in a burst access and is disposed at a front stage, and a high-speed random accessible memory disposed at a rear stage,

only said rear-stage memory is normally used,

when said rear-stage memory is full of packet data, the packet data are temporarily stored in said front-stage memory, and

the packet data are transferred back to said rear-stage memory when a free area

comes out.

12.(original): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a large-capacity low-speed access memory disposed in parallel at a rear stage,

a writing operation to said rear-stage memory is effected in parallel from said front-stage memory, and

a reading operation from said rear-stage memory is effected by selecting only a queue memory with no conflict.

13.(original): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a queue memory using a large-capacity memory that is high-speed accessible only when in a burst access and disposed at a rear stage,

a writing operation to said rear-stage memory is effected batchwise just when a plurality of packets are accumulated in said front-stage memory, and

the plurality of packets are read batchwise from said rear-stage memory.

14.(original): A packet switch comprising:

an input buffer memory unit having a logic queue corresponding to an output line;

a control module for a first pointer indicating a scheduling start input line;

a control module for a second pointer indicating a scheduling start output line of scheduling target outlines;

a request management control module for retaining transmission request data about a desired output line;

a scheduling processing module for starting a retrieval from within plural pieces of transmission request data from the output line indicated by the second pointer, and selecting an output line that is not ensured by other input lines;

a packet buffer memory unit for temporarily storing a plurality of fixed-length packets and sequentially outputting the fixed-length packets;

a common switch unit for switching the fixed-length packets outputted from said packet buffer memory unit; and

an address management unit for performing an address management of said packet buffer memory unit,

wherein said packet buffer memory executes time-division-multiplexing of the fixed-length packets of the plurality of input lines onto one signal input line in an established manner, and includes memories disposed in parallel corresponding to every input line before

being multiplexed, and

the writing and reading to and from said respective memories are executed in parallel.

15.(previously presented): A packet switch according to claim 11, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

16.(previously presented): A packet switch according to claim 11, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

17.(previously presented): A packet switch according to claim 11, wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided and

the switching can be thereby done when in maintenance and in fault.

18-22 (cancelled):

23.(previously presented): A packet switch according to claim 2, wherein said packet buffer memory unit has a large-capacity memory that is high-speed accessible only when in a burst access and is disposed at a front stage, and a high-speed random accessible memory disposed at a rear stage,

only said rear-stage memory is normally used,

when said rear-stage memory is full of packet data, the packet data are temporarily stored in said front-stage memory, and

the packet data are transferred back to said rear-stage memory when a free area comes out.

24.(previously presented): A packet switch according to claim 2, wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible memory disposed at a front stage, and a large-capacity low-speed access memory disposed in parallel at a rear stage,

a writing operation to said rear-stage memory is effected in parallel from said front-stage memory, and

a reading operation from said rear-stage memory is effected by selecting only a queue memory with no conflict.

25.(previously presented): A packet switch according to claim 2, wherein said packet buffer memory unit has a queue memory using a small-capacity high-speed random accessible

memory disposed at a front stage, and a queue memory using a large-capacity memory that is high-speed accessible only when in a burst access and disposed at a rear stage,

a writing operation to said rear-stage memory is effected batchwise just when a plurality of packets are accumulated in said front-stage memory, and

the plurality of packets are read batchwise from said rear-stage memory.

26.(previously presented): A packet switch according to claim 2, wherein said packet buffer memory executes time-division-multiplexing of the fixed-length packets of the plurality of input lines onto one signal input line in an established manner, and includes memories disposed in parallel corresponding to every input line before being multiplexed, and

the writing and reading to and from said respective memories are executed in parallel.

27.(previously presented): A packet switch according to claim 2, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

28.(previously presented): A packet switch according to claim 2, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

29.(previously presented): A packet switch according to claim 2, wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided, and

the switching can be thereby done when in maintenance and in fault.

30.(previously presented): A packet switch according to claim 12, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

31.(previously presented): A packet switch according to claim 12, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

32.(previously presented): A packet switch according to claim 12, wherein schedulers each including said control modules of the first and second pointers, said request management

control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided and

the switching can be thereby done when in maintenance and in fault.

33.(previously presented): A packet switch according to claim 13, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

34.(previously presented): A packet switch according to claim 13, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

35.(previously presented): A packet switch according to claim 13, wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided and

the switching can be thereby done when in maintenance and in fault.

36.(previously presented): A packet switch according to claim 14, wherein said common switch unit is based on a bit-slice architecture and has slice switches of which at least one slice switch is used as a redundant switch, and

switching to said redundant slice switch can be thereby done every time said slice switch receives maintenance and comes to a fault.

37.(previously presented): A packet switch according to claim 14, wherein said packet buffer memory unit is set dual on the input side and the output side of said common switch unit,

packet data are distributed to said packet buffer memory unit disposed on the output side along a route preset in said common switch unit, and

the switching can be thereby done when in maintenance and in fault.

38.(previously presented): A packet switch according to claim 14, wherein schedulers each including said control modules of the first and second pointers, said request management control module and said scheduling processing module, are disposed in dispersion,

a switch unit for selecting scheduling data between adjacent input buffer units among said input buffer units including said input buffer memory units, is further provided and

the switching can be thereby done when in maintenance and in fault.